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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/749,096 | 12/30/2003 | Rafael Reif | MIT-136DUS | 3177 |

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| EXAMINER | |
|---|---|
| OWENS, DOUGLAS W | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11:A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/749,096 | REIF ET AL. | |
| | Examiner | Art Unit | |
| | Douglas W. Owens | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/29/04; 7/15/04; 7/19/04; 9/3/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 17 is objected to because of the following informalities: in line 2, --to-- should be inserted between "corresponds" and "a". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 15 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 requires that the first surface of the second structure corresponds to a top surface of the second structure. Claim 14, which claim 15 depends from, requires that the first surface corresponds to a bottom surface of the second structure. The scope of the claim is vague because it is not known how the first surface can correspond to the top surface and the bottom surface. Claim 18 has the same problem.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 6, 10 – 15, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,767,009 to Yoshida et al.

Regarding claim 1, Yoshida et al. teach a multi-layer integrated semiconductor structure (Figs. 1 – 12, for example), comprising:

a first semiconductor structure (42) having a plurality of semiconductor elements associated with a first semiconductor technology (Col. 9, lines 28 – 40);

a second semiconductor structure (41) having a plurality of semiconductor elements associated with a second semiconductor signaling technology; and

an interface (4, 18) disposed to couple a first surface of the first semiconductor structure to a first surface of the second semiconductor structure, wherein the interface includes a first portion (4) adapted to provide a communication interface between the first semiconductor structure and the second semiconductor structure and a second portion (18) adapted to reduce electrical interference between the first and second semiconductor structures (Col. 7, lines 20 – 23).

Regarding claims 2 and 3, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the first portion of the interface includes an electrically conductive adhesive material (Col. 6, lines 12 – 16).

Regarding claim 4, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the second portion of the interface includes an electrically conductive adhesive material (Col. 4, lines 65 – 68; Col. 7, lines 39 – 45).

Regarding claim 5, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the electrically conductive adhesive material is grounded (Col. 4, lines 49 – 57).

Regarding claim 6, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the electrically conductive adhesive material includes on of copper, aluminum or a metal alloy (Col. 4, lines 65 – 68; Col. 5, lines 52 – 54; Col. 7, lines 39 – 45).

Regarding claim 10, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the first semiconductor signaling technology includes digital signaling related technology (Col. 9, lines 26 – 29; logic is related to digital signaling technology).

Regarding claim 11, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the second semiconductor signaling technology includes analog signaling related technology (Col. 9, lines 31 – 33).

Regarding claim 12, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the interface is adapted to adhesively couple the first surface of the first semiconductor structure to the first surface of the second semiconductor structure.

Regarding claim 13, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the first surface of the first semiconductor structure corresponds to a top surface of the first semiconductor structure.

Regarding claim 14, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the first surface of the second semiconductor structure corresponds to a bottom surface of the second semiconductor structure.

Regarding claim 16, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the first surface of the first semiconductor structure corresponds to a bottom surface of the first semiconductor structure.

Regarding claim 17, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the first surface of the second semiconductor structure corresponds to a top surface of the second semiconductor structure.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7 – 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. as applied to claim 1 above, and further in view of US Patent No. 5,940,683 to Holm et al.

Regarding claims 7 and 19, Yoshida et al. teach a multi-layer integrated semiconductor structure, wherein the second portion of the interface includes a dielectric material (8, 16). Yoshida et al. do not teach that the dielectric material is a dielectric adhesive. Holm et al. teach a dielectric (52; Col. 7, lines 59 – 62) with adhesive properties. It would have been obvious to one having ordinary skill at the time of the invention to incorporate the teaching of Holm et al. into the structure taught by Yoshida et al. since it is desirable to prevent the electro-conductive layer from peeling.

Regarding claims 8 and 9, Yoshida et al. do not teach a structure, wherein the dielectric adhesive material includes an organic or inorganic material. Holm et al. teach a dielectric adhesive that may be organic or inorganic. It would have been obvious to incorporate the teaching of Holm et al. into the structure of Yoshida et al., for reasons

discussed above. Additionally, it is desirable to use materials that are well suited for the intended use.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens
Examiner
Art Unit 2811